Amendments to the Claims

1. (currently amended): A lateral IGFET device comprising:

a semiconductor substrate having a first conductivity type;

a region of semiconductor material comprising alternating layers of first and second conductivity type material deposited over the semiconductor substrate and having a first major surface, the region of semiconductor material further including a top layer of the first conductivity type formed adjacent the first major surface and one of the alternating layers of the second conductivity type formed adjacent and below the top layer;

a drain region of the second conductivity type extending from the first major surface into at least a portion of the region of semiconductor material and adjoining at least a portion of the alternating layers;

a body region of the first conductivity type formed in a portion of the region of semiconductor material and extending from the first major surface partially into the top layer;

a first source region formed in the body region; ~~and~~

a trench gate structure formed in a portion of the region of semiconductor material and adjoining the alternating layers, the body region and the first source region, wherein the trench gate structure controls a sub-surface channel region; and

a surface gate structure including a gate dielectric layer formed overlying the first major surface and a gate electrode layer overlying the gate dielectric layer, wherein the surface gate structure extends over the first source region and controls conduction in a surface channel region.

2. (original): The device of claim 1 wherein in the drain region comprises a trench filled with a doped polycrystalline material.

3. (original): The device of claim 1 wherein the trench gate structure is filled with a doped polycrystalline material of the second conductivity type, and wherein the trench gate structure extends from the first major surface adjacent the source region and a portion of the body region into the region of semiconductor material, and wherein the trench gate includes a first gate dielectric layer formed at least on sidewall surfaces of the trench gate structure.

4. (currently amended): The device of claim 3 further comprising a first doped region of the second conductivity type formed ~~adjacent~~ adjoining a portion of the sidewall surfaces and portions of ~~adjacent~~ the alternating layers and extending into the semiconductor region below the body region.

Claim 5 (cancelled).

6. (original): The device of claim 1 wherein a lower portion of the trench gate structure terminates within the semiconductor substrate.

Claim 7 (cancelled).

8. (previously presented) The device of claim 1 wherein the top layer is thicker than adjacent layers in the region of semiconductor material.

9. (currently amended) The device of claim [[5]] 1 further comprising a ~~diffused~~ drain extension region of the second conductivity type formed in the top layer and between the body region and the drain region and further contacting the drain region.

10. (currently amended) A lateral MOSFET device comprising:

a semiconductor substrate;

a region of semiconductor material including a plurality of alternating layers of first and second conductivity semiconductor material formed ~~over~~ overlying the semiconductor substrate and having a major surface;

a trench drain structure formed in the region of semiconductor material;

a body region of the first conductivity type formed in the region of semiconductor material;

a source region of the second conductivity type formed in the body region;

a trench gate structure formed in the region of semiconductor material adjoining at least a portion of the alternating layers, the body region and the source region, wherein the trench gate structure controls a sub-surface channel region; and

a surface gate structure including a gate dielectric layer and a gate conductive portion formed overlying the major surface and adjacent the body region and the source region, wherein the surface gate structure controls a surface channel region.~~;~~

~~a body region of first conductivity type formed adjacent the trench gate structure and the surface gate structure; and~~

~~a source region of the second conductivity type formed in the body region.~~

11. (currently amended) The lateral MOSFET device of claim 10 further comprising ~~a diffused drain extension~~ an extended drain region of the second conductivity type formed in a portion of the region of semiconductor material and extending from the major surface, and a top region of the first conductivity type formed in ~~within a portion of~~ the extended drain region. ~~diffused drain extension region~~.

12. (previously presented): The lateral MOSFET device of claim 10 further comprising a doped region of the second conductivity type formed in the region of semiconductor material adjacent a portion of the trench gate structure and below the body region.

13. (original): The lateral MOSFET device of claim 10 wherein the region of semiconductor material includes a layer of the first conductivity type at the major surface, and wherein the layer has a thickness greater than adjacent layers within the region of semiconductor material.

14. (original): The lateral MOSFET device of claim 10 wherein at least a portion of the alternating layers within the region of semiconductor material extend between the trench drain structure and the trench gate structure.

15. (original): The lateral MOSFET device of claim 10 wherein the trench drain structure includes a trench filled with a polycrystalline semiconductor material having the second conductivity type.

16. (original): The lateral MOSFET device of claim 10 wherein the trench gate structure extends further into the region of semiconductor material than the trench drain structure.

17. (previously presented) An insulated gate FET structure comprising:

alternating layers of first and second conductivity type material forming a semiconductor region;

a trench gate structure formed in the alternating layers, wherein the trench gate structure controls a sub-surface channel region;

a body region of the first conductivity type formed in the semiconductor region adjacent the trench gate structure;

a drain region of the second conductivity formed in the semiconductor region and spaced apart from the trench gate structure and extending into the alternating layers;

a source region of the second conductivity type formed in the body region and adjacent to the trench gate structure; and

a doped region of the second conductivity type formed along a sidewall of the trench gate structure and extending into the semiconductor region below the body region.

18. (original): The insulated gate FET structure of claim 17 wherein the drain region comprises a trench filled with a polycrystalline semiconductor material.

19. (original): The insulated gate FET structure of claim 18 wherein the trench gate structure extends into the alternating layers deeper than the drain region.

20. (original): The insulated gate FET structure of claim 17 wherein the trench gate structure controls a plurality of sub-surface channel regions.

21. (previously presented): The insulated gate FET structure of claim 17 further comprising:

a top layer of the second conductivity formed over one of the alternating layers of the first conductivity type to form an upper major surface of the semiconductor region, wherein the top layer is thicker than the alternating layers of first and second conductivity type;

an extended drain region of the second conductivity type formed in a portion of the top layer and extending partially into the top layer from the upper major surface; and

a surface gate portion including a gate dielectric layer overlying the upper major surface of the semiconductor region and a gate conductive portion overlying the gate dielectric portion, wherein the surface gate portion controls a channel for conducting current at the upper major surface.